BROAD-BRAND MPSK SPREAD SPECTRUM COMMUNICATIONS RECEIVER WITH CARRIER RECOVERY AND TRACKING USING CORRELATION TECHNIQUES

RELATED APPLICATIONS

The subject application claims the priority of provisional patent application nos. 60/098,679 and 60/098,680, both filed on September 1, 1998.

FIELD OF THE INVENTION

This invention relates generally to spread spectrum communications systems. In particular the disclosed apparatus and method for carrier recovery in MPSK modulated systems are based on correlation techniques.

BACKGROUND OF THE INVENTION

Communication systems exist in various forms. Generally speaking, a communication system is designed to transmit information-embedding signals from a source to a destination. A communication system usually consists of three components: a transmitter, a channel and a receiver. The function of the transmitter is to process (also known as modulate) the information data into such a form that it can be transmitted through a channel. The channel provides a physical medium for signal transmission between the transmitter and the receiver. Examples of a channel are coaxial cable, optical fiber, and the air. A practical channel usually distorts the signal by addition of noises and time delay when the signal passes through it. The function of the receiver is to receive the transmitted signal and process (also known as demodulate) it to obtain the original information data. Since the signal received from a practical channel is usually distorted and delayed, the receiver requires mechanisms such as equalization, synchronization and so on to assist the data demodulation.

One type of communication systems is the mobile communication system, in which the signal is transmitted in the form of electromagnetic waves and the transmission medium is the air. The mobile phone communication system is a typical example of this type of communication system.

One type of mobile communication systems is Code Division Multiple Access (CDMA) system, which uses spread spectrum techniques. In this type of system the frequency bandwidth of the transmitted signal is much larger than the information bandwidth. Spread spectrum systems perform better in the presence of narrow band

noise interference and multiple user interference. Direct Sequence Code Division Multiple Access (DS-CDMA) is one of the CDMA types. In a DS-CDMA system the transmitter spreads the data stream using a given spreading code in the time domain. Orthogonal codes are often employed among different users to minimize multi-user interference. The received signal is correlated with the user spreading code so that only the desired user signal is enhanced while signals from other users are de-emphasized. In this way users can share the same time and frequency slot.

Various modulation schemes can be used in DS-CDMA systems. One of the commonly used modulations is Multiple Phase Shift Keying (MPSK), in which the serial data is grouped into $\log_2$M-bit symbols. The well known binary phase shift keying (BPSK) and quadrature phase shift keying are particular ones of MPSK, where M=2 and M=4, respectively. Each information data bit is modulated with a pseudo-noise code (PN code) of length N. The spreaded data symbols are up-converted and transmitted by a carrier of frequency f_c.

BRIEF DESCRIPTION OF THE EMBODIMENTS

FIG. 1 is the block diagram of the proposed communication system;
FIG. 2 is the block diagram of the transmitter of FIG. 1;
FIG. 3 is the block diagram of the differential encoder of FIG. 2;
FIG. 4 is the block diagram of the PN-modulator of FIG. 2;
FIG. 5 is the block diagram of the carrier tracking subsystem of FIG. 1;
FIG. 6 is the block diagram of the frequency down-converter of FIG. 5;
FIG. 7 is the block diagram of the X-correlator of FIG. 5;
FIG. 8 is the block diagram of the VCO loop of FIG. 5;
FIG. 9 is the block diagram of the frequency generator of FIG. 5;
FIG. 10 is the block diagram of the synchronization subsystem of FIG. 1 and
FIG. 11 is the block diagram of the data demodulation subsystem of FIG. 1.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the structure of the proposed communication system. The system comprises a transmitter 101, a channel 120 and a receiver 102. The receiver comprises three subsystems: the synchronization system 103, the carrier tracking system 104 and the data demodulation system 105. The information data is fed to the transmitter 101, where it is processed and transmitted as the signal 121 through the channel 120. The transmitted signal which has passed through the channel 120

is denoted as signal 107. Receiver 102 receives the signal 107 and passes it on to the three subsystems 103, 104 and 105. The disclosed apparatus for carrier recovery is employed in the carrier tracking subsystem 104. The said carrier tracking subsystem 104 supplies control signal 112 to said synchronization subsystem 103 and adjusted frequency 113 to said data demodulation subsystem 105. The synchronization subsystem 103 supplies synchronized clock 114 as a synchronization signal to the data demodulation subsystem 105. With the adjusted frequency 113 from said carrier tracking subsystem 104 and the synchronized clock 114 from said synchronization subsystem 103, the data demodulation subsystem 105 demodulates the received signal 110 into information data 115.

FIG. 2 shows the detailed structure of the transmitter 101. It essentially comprises a serial-to-parallel converter 201, a differential encoder 202, a PN modulator 203, a PN sequence generator 204, two lookup tables storing the cosine and sine values of different phases, namely, the Acm table 205 and the Asm table 206, respectively, two low pass filters 207 for the I-channel and 208 for the Q-channel, a carrier table 209, an orthogonal phase shifter 210, two multipliers 211 for the I-channel and 212 for the Q-channel and an adder 213. Said serial-to-parallel converter 201 groups every m bits of the serial data 106 into one symbol 214 and each symbol is mapped into $2^m=M$ different phases. The m-bit symbols 214 go through the differential encoder 202. The output 215 of said differential encoder 202 is fed to said PN modulator 203, in which these phases are modulated by the PN-sequence 217 supplied by said PN sequence generator 204. The m-bit outputs 218 of said PN modulator 203 are used as addresses 219 and 220 for looking up tables Acm table 205 and Asm table 206, which store the cosine and sine values of M different phases, respectively. Low pass filters 207 and 208 limit the bandwidth of the I- and Q-path signals 221 and 222 before they modulate the carrier 225 from the carrier table 209. The I- and Q-path signals 227 and 228 are combined in adder 213 and transmitted as MDPSK signals 121 for further up-conversion.

FIG. 3 shows the structure of said differential encoder 202 of FIG. 2. It essentially comprises an m-bit modulo adder 301 and an m-bit D flip flop 302. The m-bit symbol 303 is fed to said adder 301, wherein it is added with the successive result 305 of said adder 301, which was delayed by said D flip flop 302 for one symbol duration. The addition operation is modulo-M based, where M represents the number of the phases, herein specifically $2^m=M$.

FIG. 4 shows the structure of said PN modulator 203 of FIG. 2. The PN sequence 406 of K chips in length comes from said PN sequence generator 204 of FIG. 2. Each chip is multiplied at multiplier 403 with M/2 from register 401. The multiplication result 405 is supplied to the adder 402, wherein it is added with the symbol 404 from said differential encoder 202 of FIG. 2. The addition operation is M-modulo based, where M represents the number of phases. The addition result 408 is used as addresses for looking up said tables 205 and 206 of FIG. 2.

FIG. 5 shows the block diagram of said carrier tracking subsystem 104 of FIG. 1. The MDPSK signal 109 is received and split into two symmetric paths, the positive one 511 and the negative one 512. The MDPSK signal 511 is down-converted at the down-converter 501 into base-band I- and Q-path signals 513 and 514, which are supplied to the X-correlator 503, where they are correlated with the local PN-sequence. The output 517 of the X-correlator 503 is fed to the VCO loop 505 as the positive control signal. Signal 517 also acts as said control signal 112 for said synchronization subsystem 103 of FIG. 1. The negative path executes the same operations except that the MDPSK signal 512 is down-converted by the orthogonal carriers 522, the frequency of which is different from that of the positive path. The down-converter 502 supplies the base-band I- and Q-path signal 515 and 516 to the X-correlator 504. The signal 518 obtained from the X-correlator 504 is fed to the VCO loop 505 as the negative control signal. The VCO loop provides a clock signal 519 to the frequency generator 506, which generates three different frequencies, the adjusted carrier frequency 520, the frequency 521 with a positive offset to the frequency 520 and the frequency 522 with the same offset but negative to the frequency 520. The frequency 520 is used as the control signal 113 for the data demodulation subsystem 105 of FIG. 1.

FIG. 6 shows the block diagram of said down-converters 501 and 502 of FIG. 5. The structure is illustrated with down-converter 501 as follows. The structure of said down-converter 502 is the same. The down-converter includes two multipliers 601 and 602 and a phase shifter 603. The MPSK signal 510 is received and split into two paths 610 and 611. Said frequency signal 521 from said frequency generator 506 of FIG. 5 is fed to said down-converter 501 as a carrier for down-converting the path signal 610 at the multiplier 601, generating the base-band I-path signal 513. Said frequency signal 521 is shifted 90° by the phase shifter 603 and supplied to multiplier 612 for down-converting the path signal 611, generating the base-band Q-path signal 514. Said two base-band path signals 513 and 514 are

supplied to the X-correlator 503 of FIG. 5. The base-band I- and Q-path signals 515 and 516 from down-converter 502 are supplied to said X-correlator 504 of FIG. 5.

FIG. 7 shows the block diagram of said X-correlators 503 and 504 of FIG. 5. The structure is illustrated with said X-correlator 503 as follows. The structure of said X-correlator 504 is the same. The base-band I- and Q-path signals 513 and 514 are supplied to two parallel shift registers 701 and 702. Outputs of said two parallel shift registers 701 and 702 are fed to the correlators 703 and 704, respectively, where they are correlated with the local PN-sequence from the PN-generator 705. The correlation results 715 and 716 are squared at 706 and 707. The results 717 and 718 are combined at adder 708 into signal 719. Said signal 719 is compared with a preset threshold 710, which ensures that the output 517 of the correlator 503 is the correlation peak value. The correlation peak value 518 of the other MPSK signal path 512 is obtained from said X-correlator 504. The two correlation peak values 517 and 518 are supplied to said VCO loop 505 of FIG. 5 as the positive and negative control signals, respectively. Signal 719 is also used as said control signal 112 for the synchronization subsystem 103 of FIG. 1.

FIG. 8 shows the block diagram of said VCO loop 505 of FIG. 5. Said correlation signals 517 and 518 of FIG. 7 act as positive and negative signals for said VCO loop 505. The difference 810 between said correlation signals 517 and 518 is amplified by amplifier 805 with gain G. The amplified signal 811 passes through the low pass filter 802. The output signal 812 of said low pass filter 802 is the error control signal for the voltage controlled oscillator (VCO) 801. Said VCO 801 generates the adjusted frequency clock 519, which is fed to said frequency generator 506 of FIG. 5 for generating the three said adjusted frequencies.

FIG. 9 shows the block diagram of said frequency generator 506 of FIG. 5. The VCO loop output clock signal 519 controls the counter 901 for generating addresses to look up ROM tables 902, 903 and 904. Said table 903 stores the values of a cosine waveform of the frequency f_c, said table 902 stores the value of the cosine waveform of frequency f_c+D and said table 904 stores the value of the cosine waveform of the frequency f_c-D, where D represents a positive frequency offset to the frequency f_c. Outputs 912, 913 and 914 of said three ROM tables 902, 903 and 904 pass through digital-analogue-converters (D/A) 905, 906 and 907 and are fed to said down-converter 501, said data demodulation subsystem 105 and said down-converter 502, respectively.

FIG. 10 shows the block diagram of said synchronization subsystem 103 of FIG. 1. It comprises N registers R_1 1001, R_2 1002, ..., $R_{(N-1)/2}$ 1003, ..., R_N 1005, and a subtractor 1004, where N represents an odd number. Said signal 112 from the X-correlator 503 of FIG. 7 is sampled N times per chip and the N sampled values are stored in said N registers R_1, R_2 , ..., $R_{(N-1)/2}$, ..., R_N. The difference signal 1012 between the left most value in R_1 1001and the right most value in R_N 1005 represents the phase error of the chip clock. The middle value in $R_{(N-1)/2}$ 1003 is used for coarse synchronization of the symbol clock.

FIG. 11 shows the block diagram of said data demodulation system 105 of FIG. 1. Said MDPSK signal 110 from the transmitter is down-converted at down-converter 1101 by said adjusted carrier 520 from the frequency generator 506 of FIG. 5. The down-converted signal 1120 is split into two paths, which pass through two matched filters 1102 and 1103, respectively. The outputs of said matched filters 1102 and 1103 are delayed for one data bit at 1104 and 1105 to form signals 1129 and 1130. Four multipliers 1106, 1107,1108 and 1109 are employed. Signals 1129 and 1121 are multiplied at 1106 to form signal 1123, signals 1121 and 1130 are multiplied at 1107 to form 1124, signals 1122 and 1129 are multiplied at 1108 to form 1125, and 1122 and 1130 are multiplied at 1109 to form 1126. Signal 1123 and 1126 are combined at adder 1110 to form signal 1127. Signal 1124 is subtracted from 1125 at subtractor 1111 to form 1128. Said signals 1127 and 1128 are normalized and used for looking up table values at 1112, which stores phases of the MPSK modulation. The result obtained from 1112 is the demodulated data 115 of FIG. 1.